DOCKET NO. 99-039/RCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	:	Sheldon Aronowitz, Valeric Sukharev, John Haywood, James P. Kimball, Helmut Puchner, Ravindra Manohar Kapre, and Nicholas Eib
Appl. No.	:	09/464,297
Filed:	:	December 15, 1999
Title	:	PROCESS FOR ETCHING A CONTROLLABLE THICKNESS OF OXIDE ON AN INTEGRATED CIRCUIT STRUCTURE ON A SEMICONDUCTOR SUBSTRATE USING NITROGEN PLASMA AND AN RF BIAS APPLIED TO THE SUBSTRATE
Grp./ A.U.	:	1765
Examiner	:	Lan Vinh
Docket No.	:	99-039/RCE

RULE 131 DECLARATION OF JOHN P. TAYLOR, PATENT ATTORNEY FOR THE ASSIGNEE, LSI LOGIC CORPORATION

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

I, John P. Taylor, (Declarant) do declare as follows:

1) That the Declarant is an attorney at law, registered to practice as a patent attorney by the United States Patent and Trademark Office;

2) That the Declarant has been engaged to represent LSI Logic Corporation before the United States Patent and Trademark Office for over ten years;

3) That on September 8, 1999, the Declarant received from the Intellectual Property Department of the LSI Logic Corporation a facsimile transmission of an authorization from the LSI Logic Corporation (Exhibit A) to prepare a patent application on the subject matter of their patent docket 99-039;

4) That the Declarant advised LSI Logic that the Declarant might not be able to complete the preparation of the first draft of a patent application within the normal six week period allotted;

5) That LSI Logic then reset the start date for work to commence on the case by 10/4 of 1999, (as also shown in Exhibit A);

6) That transmitted with this authorization was a seven page disclosure (Exhibit B- first four pages and Exhibit C - last three pages) which included the dated and witnessed signatures of all seven of the inventors on each of the first four sheets of the disclosure as shown in Exhibit B, with the dates varying from February 8, 1999 to February 11, 1999;

7) That the last three sheets of the seven page disclosure, marked as Exhibit C, comprise a report of experimental results;

8) That the first page of this report (Exhibit C) bears the title: **APPLICATION OF REMOTE NITROGEN PLASMAS TO CONTROLLABLY ETCH GATE OXIDE**, and also lists and identifies as Inventors, just after the title, all seven of the inventors listed in U.S. Patent Application Serial No. 09/464,297;

9) That each of the three pages comprising this report (Exhibit C), bears, at the bottom of the page the following legend: **LSI LOGIC CONFIDENTIAL 02/05/99;**

10) That the three page report (Exhibit C) contains the following statements:

a) (Exhibit C, page 1) "The **experimental** conditions were that 4.5 nm of oxide was grown, the wafer was masked and quadrants of the wafer were sequentially exposed to different nitrogen plasma conditions. One set involved **only variations in bias power with all other parameter fixed**:" (emphasis added)

b) (Exhibit C, pages 1-2) "It was found that **a *specific* amount of oxide was etched for each bias power setting**. As an example, the oxide thickness was reduced to 3.0 nm when the bias power was set at 15 w while the oxide thickness was reduced to 1.7 nm when the bias power was set at 30 w. The **uniformity across the wafer was very tight.**" (bold emphasis added, italized emphasis in original)

c) (Exhibit C, page 2) "It was found that **decreasing the ICP value from 500 w to 250 w**, while all other factors were kept constant, **did not materially change etch behavior**." (emphasis added)

11) That from the above bolded statements in Exhibit C, the Declarant believes that Exhibits B and C not only serve as a record of conception as of February, 1999, but further serve as a record of a reduction to practice of the invention on or before February 5th of 1999;

12) That the disclosure was received by the LSI Logic Corporation Intellectual Property Department on 1999/02/12 as shown in Exhibit D;

13) That the disclosure was sent to a LSI Logic Corporation Intellectual Property Department attorney for review on 1999/03/03, as also shown in Exhibit D;

14) That the disclosure was received back from the LSI Logic Corporation Intellectual Property Department attorney with his 1st review on 1999/03/04, as also shown in Exhibit D;

15) That the disclosure was sent to a LSI Logic technical reviewer for review on 1999/05/11, as also shown in Exhibit D;

16) That the disclosure was sent back to the LSI Logic Corporation Intellectual Property Department attorney for a final review on 1999/07/24, as also shown in Exhibit D;

17) That the disclosure was received back from the technical reviewer on 1999/07/24, as also shown in Exhibit D, with the notation APPROVED thereon;

18) That the disclosure was deferred on 1999/07/26, as shown in Exhibit D;

19) That the disclosure and the final review of the LSI attorney were received on 1999/07/26, as further shown in Exhibit D;

20) That between 1999/07/26 and 1999/09/08 a decision was made by LSI Logic Corporation to file the application, as inferred by Exhibit D;

21) That the disclosure was then sent to the Declarant with the authorization to prepare a patent application;

22) That Declarant contacted one of the inventors, Sheldon Aronowitz, by telephone concerning a proposed trip to San Jose to discuss Docket 99-039, as shown on second page of October 1999 telephone bill (Exhibit E);

23) That Declarant met with the inventors during a subsequent trip to San Jose on October 11-12, 1999 as shown on Declarant's October 11-12, 1999 trip expense report (Exhibit F);

24) That thereafter during the period between October 13, 1999 and November 5, 1999, the Declarant prepared the first draft of a patent application for Docket 99-039, as evidenced by three telephone calls to the inventors in San Jose listed on page 2 of Declarant's November telephone bill (see page 3 of November, 1999 telephone bill (Exhibit G));

25) That on November 5, Declarant mailed a letter to the inventors (Exhibit H) forwarding to them the first draft of a patent application containing the contents of Docket 99-039 for their review (pages 1, 11, 12, and a flowsheet of that first draft comprise Exhibit I);

26) That further telephone calls were made to the inventors on November 11 and 12th (as shown on pages 3 and 4 of Exhibit G);

27) That Declarant made a further trip to San Jose on December 3rd to review the first draft of the invention to the inventors (see expense report labelled Exhibit J);

28) That on December 4, 1999 Declarant sent to attorney Ralph Veseli of the Intellectual Property Department of LSI Logic, by Federal Express, the patent application in final form for filing in the USPTO; copies of the drawings, and copies of the declaration and assignee to be executed by the inventors (see Declarant's letter marked Exhibit K and the copy of the Federal Express receipt marked Exhibit L);

29) That on December 6, 1999, Declarant mailed a second letter to Ralph Veseli (Exhibit M) enclosing the remaining papers needed to file the application in the USPTO after execution by the inventors of the previously sent Declaration and Assignment papers. (Declarant's normal practice was to send the executed patent application to the USPTO from his office, but due to the impending death of Declarant's mother (who subsequently died in Indiana on December 20th) and in view of Declarant's desire to travel to Indiana to visit with his mother before her passing and to be with her when she died, the LSI Logic attorney agreed to handle the filing of the application in the USPTO on December 15, 1999).

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

01/22/04
Date

John P. Taylor